

**AMENDMENTS TO THE CLAIMS**

1. (Currently amended) A method of manufacturing a semiconductor device, comprising ~~the steps of~~:

(a) sequentially forming a tunnel oxide film, a first polysilicon film and a pad nitride film on a semiconductor substrate;

(b) etching portions of the pad nitride film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate by means of a patterning process to form a trench within the semiconductor substrate;

(c) depositing an oxide film on the entire structure including the trench and then ~~planarization~~ planarizing the oxide film so that the pad nitride film is exposed;

(d) etching the pad nitride film to form an oxide film protrusion;

(e) depositing a second polysilicon film on the entire structure and then ~~planarization~~ planarizing the second polysilicon film so that the oxide film protrusion is exposed, thereby forming a floating gate having the second polysilicon film formed on the first polysilicon film; and

(f) etching a part of the exposed oxide film protrusion to ~~form a floating gate~~ improve a coupling ratio, and then forming a dielectric film and a control gate.

2. (Original) The method as claimed in claim 1, wherein the first polysilicon film is formed in thickness of 200 ~ 1000Å using SiH<sub>4</sub> or Si<sub>2</sub>H<sub>6</sub> and PH<sub>3</sub> gas by means of CVD, LPCVD, PECVD or APCVD method at a temperature of 530 ~ 680°C under a pressure of 0.1 ~ 3.0torr.

3. (Original) The method as claimed in claim 1, wherein the tunnel oxide film is deposited in thickness of 85 ~ 110Å at a temperature of 750 ~ 800°C by means of wet oxidization and is then experienced by annealing using N<sub>2</sub> at a temperature of 900 ~ 910°C for 20 ~ 30minutes.

4. (Currently amended) The method as claimed in claim 1, further comprising the ~~step of before the step~~ (a), implementing an ion implantation process to form a well within the semiconductor substrate.

5. (Currently amended) The method as claimed in claim 1, further comprising the ~~steps of: between the step (b) and the step (c);~~

implementing a sidewall oxidization process for compensating for damage of the semiconductor substrate that occurred upon formation of the trench;

implementing a rapid thermal process for making rounded the corner of the trench;  
and

depositing a high temperature oxide film on the entire structure ~~along the step~~ and then implementing a densification process at high temperature.

6. (Currently amended) The method as claimed in claim 1, further comprising the ~~step of~~ between the ~~step (d) and the step (e)~~, implementing a wet cleaning process for preventing the tunnel oxide film from being lost, to remove the first polysilicon film in thickness of about 100 ~ 700Å.

7. (Currently amended) The method as claimed in claim 1, wherein ~~the step (e)~~ comprises ~~the steps of~~:

depositing a second polysilicon film on the entire structure;

depositing a buffer layer on the second polysilicon film for reducing an top surface ~~step of the second polysilicon film on the second polysilicon film~~; and

implementing a chemical mechanical polishing (CMP) process using the oxide film protrusion as a stop layer to smooth the buffer layer and the second polysilicon film.

8. (Original) The method as claimed in claim 7, wherein the buffer layer is at least one of a PE-TEOS layer, a PE-Nit layer, a PSG layer and a BPSG layer, which are formed by a PE-CVD method.

9. (Original) The method as claimed in claim 1, wherein the second polysilicon film is formed in thickness of 800 ~ 2500Å using SiH<sub>4</sub> or Si<sub>2</sub>H<sub>6</sub> and PH<sub>3</sub> gas by means of a CVD, LPCVD, PECVD or APCVD method at a temperature of 530 ~ 680°C under a pressure of 0.1 ~ 3.0torr.

10. (New) A method of manufacturing a semiconductor device, comprising:

(a) sequentially forming a tunnel oxide film, a first polysilicon film and a pad nitride film on a semiconductor substrate;

(b) etching portions of the pad nitride film, the first polysilicon film, the tunnel oxide film and the semiconductor substrate by a patterning process to form a trench within the semiconductor substrate;

(c) depositing an oxide film on the entire structure including the trench and then planarizing the oxide film so that the pad nitride film is exposed;

(d) etching the pad nitride film to form an oxide film protrusion;

(e) depositing a second polysilicon film on the entire structure and then removing the second polysilicon film on the oxide film protrusion by means of chemical mechanical polishing (CMP) process, thereby forming a floating gate having the second polysilicon film formed on the first polysilicon film; and

(f) removing a thickness of the exposed oxide film protrusion by a pre-treatment cleaning process to improve a coupling ratio, and then forming a dielectric film and a control gate.

11. (New) The method as claimed in claim 10, wherein the first polysilicon film is formed in thickness of 200 ~ 1000Å using  $\text{SiH}_4$  or  $\text{Si}_2\text{H}_6$  and  $\text{PH}_3$  gas by means of CVD, LPCVD, PECVD or APCVD method at a temperature of 530 ~ 680°C under a pressure of 0.1 ~ 3.0torr.

12. (New) The method as claimed in claim 10, wherein the tunnel oxide film is deposited in thickness of 85 ~ 110Å at a temperature of 750 ~ 800°C by means of wet oxidization and is then annealed using  $\text{N}_2$  at a temperature of 900 ~ 910°C for 20 ~ 30 minutes.

13. (New) The method as claimed in claim 10, further comprising before (a), implementing an ion implantation process to form a well within the semiconductor substrate.

14. (New) The method as claimed in claim 10, further comprising between (b) and (c):

implementing a sidewall oxidization process for compensating for damage of the semiconductor substrate that occurred upon formation of the trench;

implementing a rapid thermal process for making rounded the corner of the trench;  
and

depositing a high temperature oxide film on the entire structure ~~along the step~~ and then implementing a densification process at high temperature.

15. (New) The method as claimed in claim 10, further comprising between (d) and (e), implementing a wet cleaning process for preventing the tunnel oxide film from being lost, to remove the first polysilicon film in thickness of about 100 ~ 700Å.

16. (New) The method as claimed in claim 10, wherein (e) comprises:

depositing a second polysilicon film on the entire structure;

depositing a buffer layer on the second polysilicon film for reducing a top surface of the second polysilicon film; and

implementing the chemical mechanical polishing (CMP) process using the oxide film protrusion as a stop layer to smooth the buffer layer and the second polysilicon film.

17. (New) The method as claimed in claim 16, wherein the buffer layer is at least one of a PE-TEOS layer, a PE-Nit layer, a PSG layer and a BPSG layer, which are formed by a PE-CVD method.

18. (New) The method as claimed in claim 10, wherein the second polysilicon film is formed in thickness of 800 ~ 2500Å using  $\text{SiH}_4$  or  $\text{Si}_2\text{H}_6$  and  $\text{PH}_3$  gas by means of a CVD, LPCVD, PECVD or APCVD method at a temperature of 530 ~ 680°C under a pressure of 0.1 ~ 3.0torr.

19. (New) The method as claimed in claim 10, wherein the pre-treatment cleaning process is performed using HF or buffered oxide etchant.